Claims

What is claimed is:

1. A non-volatile memory array having rows and columns of memory cells, each cell comprising:

first and second non-volatile memory transistors symmetrically arranged in a common substrate having a planar surface and sharing a common electrode, each memory transistor having a first portion of a single layer of poly electrically floating over the substrate in a configuration having a step that extends below the planar surface of the substrate and separated from the substrate by an oxide layer thereby allowing the floating poly layer to act as a floating gate and having a capacitor connected thereto configured to act as a control electrode, the floating gate capable of electrically communicating with a subsurface electrode through the oxide layer;

first and second word lines outward of the first and second memory transistors, respectively, the word lines shared by a plurality of memory cells in the same column, a bit line transverse to the word lines in capacitive relation therewith and also in capacitive relation to the floating gates of the first and second memory transistors; and

first and second control lines, each being a plate of the capacitor associated with each memory transistor.

2. The array of claim 1 wherein the common electrode is a subsurface source or drain electrode, the symmetric arrangement of the memory cells being relative to the common electrode.

3. The array of claim 1 wherein the first and second control lines are phased thereby providing momentary exclusive use of the common electrode by one of the memory cells.

4. The array of claim 1 wherein the bit line is diffused into the substrate.

5. The array of claim 1 wherein the word lines are disposed above the substrate and separated therefrom by an oxide layer.

6. The array of claim 1 wherein the first and second control lines are spaced apart and co-linear.

7. The array of claim 5 wherein the first and second word lines are second portions of the single poly layer.

8. The array of claim 1 wherein said step extends below the planar surface of the substrate by a depth equal to 400 to 600 Angstroms.

9. The array of claim 1 wherein said step has top and bottom corners.

10. The array of claim 6 wherein the co-linear control lines are separated from bit lines of neighboring memory cells in the same column by a distance occupied by shallow trench isolation trenches.

11. The array of claim 6 wherein the co-linear control lines are diffused into the substrate.

12. A memory array having a plurality of memory cells, each cell comprising:

a pair of parallel word lines, each word line having a pair of first capacitors in series therewith, each first capacitor having a pair of plates;

a bit line associated with one capacitor plate of each first capacitor;

a pair of EEPROM memory transistors each having a drain, source and gate, the drain of each memory transistor connected to the one capacitor plate of each respective first capacitor, the sources of the pair of transistors mutually joined in a common electrode, and the gate of each transistor being a floating gate having a step therein for electric field concentration; and

a pair of second capacitors each having one plate associated with a control line input terminal and another plate connected to the floating gate of an EEPROM transistor.

13. The memory array of claim 12 wherein the step in each floating gate is at least partially below a silicon surface of a silicon wafer, said step having top and bottom corners.

14. The memory array of claim 12 wherein said EEPROM transistors have first portions of a single layer of poly as floating gates.

15. The memory array of claim 14 wherein said memory cells have a second portion of said single layer of poly functioning as said word lines.

16. The memory array of claim 13 wherein said bit line is diffused below the surface of said silicon wafer.

17. The memory array of claim 12 wherein said first capacitors are formed by an intersection of said word lines with said bit line.

18. The memory array of claim 12 wherein said pair of word lines, the pair of second capacitors, and the pair of EEPROM transistors are symmetrically disposed about the common electrode.

19. In an EEPROM transistor in a memory array of the EEPROM type fabricated in a silicon wafer with an oxide coating on the wafer surface, with a source, drain and floating gate, the improvement comprising a step in floating gate extending at least partially below the wafer surface and a first capacitor control element with first and second capacitor plates, the first plate connected to the floating gate.

20. The transistor of claim 19 having a second capacitor connected to a source or drain electrode.

21. The transistor of claim 19 wherein said second capacitor has plates associated with a word line and a bit line of the memory array.

22. The transistor of claim 19 wherein said step has top and bottom corners.